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Low Power Nand Gate

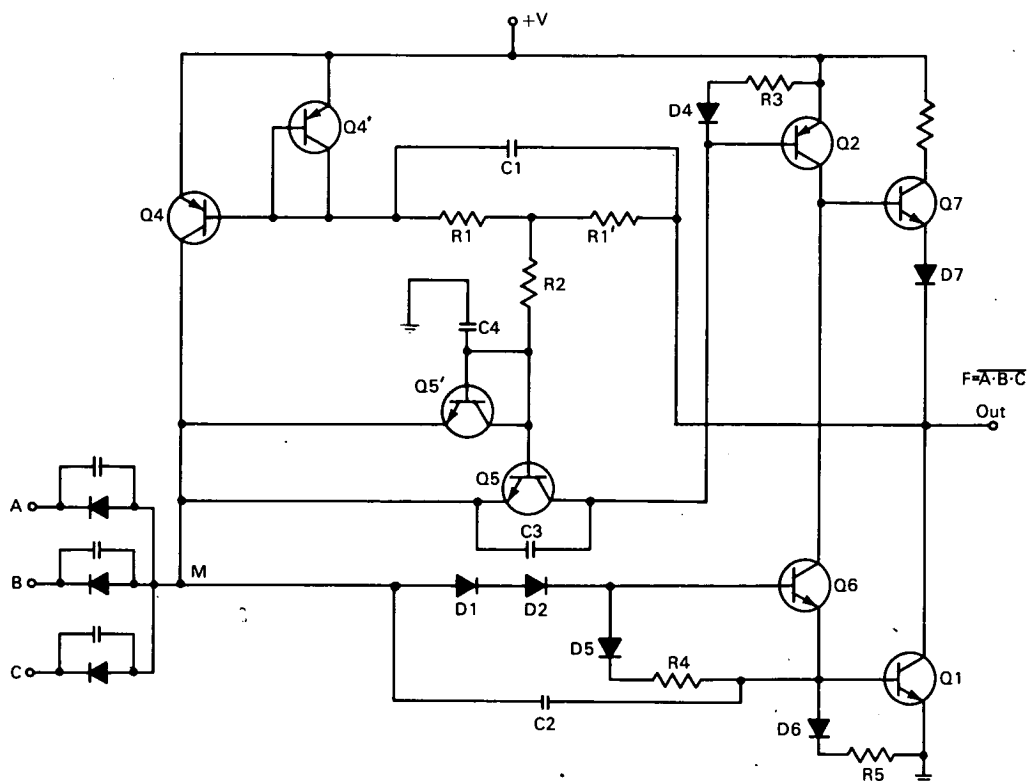


Figure 1. Low Power Nand Gate Schematic.

The problem:

Low power operation creates many problems in integrated circuit design. The rationale for achieving low power operation is the optimization of the possible trade-off conditions. If the power dissipation of a circuit is to be reduced, either the voltage or the current, or both, must be reduced. In any case, compromises must be made in the circuit gain, speed and noise immunity.

The solution:

A complementary pnp transistor, used as the load resistor, reduces the switching time and the steady state dc current, and allows for a lower supply voltage. Current limiting is achieved by a novel unity-gain transistor.

How it's done:

Figure 1 shows the scheme which provides the base current for Q2. An auxiliary transistor Q5 is con-

(continued overleaf)

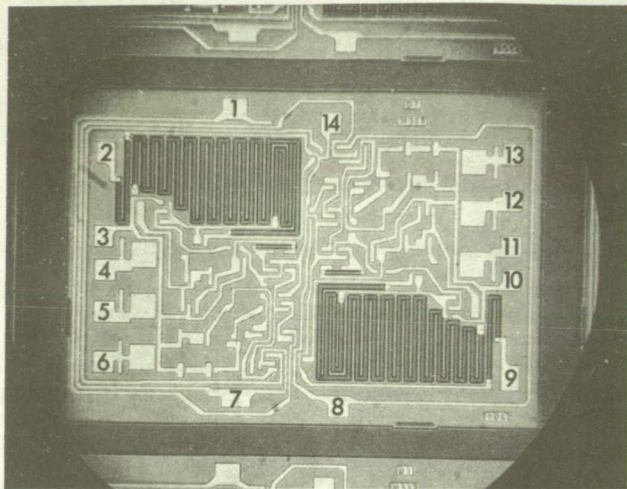


Figure 2. Physical Layout of Low Power Nand Gate.

connected between the common node M and the base of Q2. When all the inputs are at the "1" level, the base of Q5 assumes a potential lower than the emitter and cuts off Q5. When any one of the inputs is at "0" level, the node potential at M drops below that at the base of Q5 and turns on Q5 causing the base current of Q2 to flow. Q5 also serves as the initiator for starting the regenerative pnp switching action when all the inputs are at the "1" state. Once point M becomes unclamped by the input diode, the forward biased junctions of Q4 and Q5 force a current to flow into the base of Q1 through the level setting diodes and regeneration takes place.

Capacitors C1, C2, and C3 provide a low impedance charging path for the charging currents in order to

decrease the turn-off time. The resistor-diode combinations, shunting the base emitters of Q2, Q6, and Q1, maintain constant current gain and provide bleed-off paths for I_{CBO} . The collector of Q6 is connected to the base of Q7 to speed up the turnoff of Q7; Q2, aided by Q7, provides a high output current when the output is at the "1" state.

Five engineering lots of the low power Nand gate have been produced in integrated form. Two Nand gates are fabricated on a chip in Figure 2 with the dimensions of 82 mils by 117 mils. Two interconnection patterns permit resistor pull-up for a "collector OR" or complementary output operation and a complementary output with an extended input. Conventional integrated circuit processing is used to fabricate the gates with the one addition of thin-film tantalum resistors deposited on the surface of the die.

Note:

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Patent status:

No patent action is contemplated by NASA.

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